Patent

5 1A
1-28-98
C Brown

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Vora

Art Unit: 2512

Examiner: GIORDANA

Serial No. 08/654,760

Filed: 5/29/96

For: VERTICALLY INTEGRATED FLASH EEPROM FOR GREATER DENSITY AND LOWER COST

Box Amendment
Honorable Commissioner
of Patents and Trademarks
Washington, D.C. 20231

Morgan Hill, California
November 15, 1997

AMENDMENT

Dear Sir:

In response to the Office Action mailed , please amend the above identified case as follows.

IN THE DRAWINGS

Enclosed is a markup of Figures 3 and 4 for approval by the Examiner.

IN THE SPECIFICATION

At page 1, line 11, delete "appliction", and substitute --application--.

IN THE CLAIMS

1. (Amended) A nonvolatile memory cell array comprised of a plurality of EEPROM memory cells, each cell comprising:

a semiconductor substrate;

a vertical MOS transistor formed by alternating N-type and P-type doped layers